REMARKS/ARGUMENTS

Favorable reconsideration of this application in view of the following remarks is respectfully requested.

Claims 1-3, 5-10 and 12-18 are presented for examination on this application. Claims 4 and 11 have been canceled without prejudice or disclaimer. Claims 14-18 have been withdrawn from consideration. Claims 2, 3, 5, 6, 8-10, 12, and 13 were previously amended. Claims 1 and 7 have been currently amended without the introduction of any new matter to better highlight the present invention.

The outstanding Office Action includes a rejection of Claims 1-13 under 35 U.S.C. § 103(a) over what is alleged in the outstanding Action to be "Applicant's Admitted Prior Art" (AAPA) in view of Yu (U.S. Patent No. 6,225,173).

Initially, Applicants acknowledge with gratitude the discussion held with Examiner Toledo on May 6, 2003. During this discussion, Applicant's representative pointed to the seeming inconsistency at the top of page 3 of the outstanding Office Action where the second trench was referenced instead of the first trench that would actually be formed by removing the dummy gate electrode. The Examiner indicated that the references to the second trench in line 2 at the top of page 3 were unintentional and pointed out that the paragraph beginning at line 4 on this page made it clear that there was an enlarging of the width of the first trench to form the second trench that was not taught by the AAPA. The Examiner also emphasized hat Yu was relied on to teach enlarging the first trench to form the second trench.

Relative to this last point, Applicant's representative pointed out that there was no teaching to be found in either Figures 1-8 of the present application or any part of Yu as to

having the width of the first trench enlarged by the claimed amount that must be equal to or greater than the thickness of the gate insulating film to be lined.

The Examiner suggested that this limitation was not specific enough to overcome the trench enlargement taught by Yu, even though this enlargement was for a different purpose and clearly done with total disregard as to any gate insulating film width.

Applicant's representative also pointed out that Yu was unconcerned with the amount of sidewall that was removed, that Yu was not concerned with the thickness of any insulating film to be formed, and that the whole purpose of Yu was to etch the substrate 14 to form the recessed portion 48 so as to form corners 52 and 54 as illustrated in FIG. 5. While the Examiner acknowledged that forming the recessed portion 48 so as to form corners 52 and 54 as illustrated in FIG. 5 of Yu required the substrate to be etched as well as the tench sidewalls, the Examiner observed that the claim limitations then in effect did not preclude etching the substrate during trench enlargement.

Applicant's representative then suggested the present amendment to Claims 1 and 7 as to including such a limitation to preclude substrate etching as part of the enlarging of the trench to conclusively define over Yu. However, the Examiner indicated that such a limitation could not be added after final rejection as it would involve new search and consideration issues.

Accordingly, Applicant has instituted the present Request for Continued Examination (RCE) under 37 CFR §1.114 to insure entry of this Amendment and consideration of the limitation precluding substrate etching as part of the enlarging of the trench in terms of

clearly distinguishing over the reasonable teachings and suggestions of the AAPA and Yu, whether they are considered alone or together.

Before considering the outstanding obviousness rejection further, it is believed that a brief review of the present invention would again be helpful. In this respect, the invention relates to a method of making an insulated gate field effect transistor that uses a buried type gate electrode structure that avoids gate offset. In accordance with this method, a buried type gate electrode structure is formed using a dummy electrode as shown, for example, relative to Figure 12. The gate length of this dummy electrode is coincident with the final gate length as noted in the specification at page 12, lines 11-12, for example. After the trench is formed by removing the dummy electrode, this trench is broadened on both sides thereof by a predetermined width amount which is equal to or slightly greater than the thickness of the gate insulating film to be formed later. Note, for example, page 14, lines 9-15. No etching of the semiconductor substrate is involved. As shown in Figures 15 and 16, for example, the gate insulation film is formed so as to line the inner surface of the trench and a final gate electrode having the final gate length is buried therein. According to the method of manufacture, a gate structure is achieved which avoids gate offset as clearly shown in Figure 15, for example.

Turning to the rejection of Claims 1-13 under 35 U.S.C. § 103, this rejection is traversed because even if the subject matter said to be conventional is modified by the teachings of Yu, the subject matter of Claims 1-13 would not be the result of such a combination as noted above and during the above-noted discussion of May 6, 2003.

In this regard, Yu teaches the etching of substrate 14 to form the recessed portion 48 so as to form corners 52 and 54 as illustrated in FIG. 5 as noted above and during the May 6, 2003, discussion. As noted above, the present amendments to Claims 1 and 7 emphasize that the enlarging of the width of the first trench on each side of the first trench by a predetermined amount to form the second trench in the insulating film is without any etching of the semiconductor substrate which contradicts the who;e purpose of Yu that requires the substrate be etched to form the shallow source/drain extensions relied on in the outstanding Action as motivation.

In addition, Yu also teaches that his method for manufacturing ultra-shallow source/drain extensions involves first forming a buried type dummy gate 37 as shown in Fig. 3. This dummy gate 37 is removed, as shown in Fig. 4, to thereby form a first trench. While this much of the disclosure of Yu is similar to that of the present invention, Yu does not teach that the gate length of the dummy gate 37 should correspond to the final gate electrode length that will be in the second wider trench shown in FIG.5.

Moreover, as shown in Fig. 5 of Yu, the amount by which the width of the trench is increased is determined in accordance with the requisite dimension of the source/drain extensions being formed by substrate etching, now precluded by claims 1 and 7, with total disregard for increasing trench width in accordance with the thickness of the final gate insulating film, unlike the present invention.

Furthermore, in Yu, final gate electrode 36 is buried into a trench with a separator 32 and a gate insulating film 33 imposed between the gate electrode 36 and the trench. Also, Yu does not refer to the gate length but discloses that the width of a first formed spacer, that is,

spacer 42, falls within the range of 30-80 nm (col. 4, line 18), and that of a final spacer, that is, spacer 18, falls within the range of 8-10 nm (col. 5, lines 3-4). Accordingly, if the width of the trench is increased by an amount approximately equivalent to the width of the spacer 42, the final gate length is going to be greater than the gate length of the dummy gate by about 22-70 nm. That is, Yu does not teach the method of the present invention which sets the gate length of the dummy gate electrode at the predetermined length which is the final gate length.

Accordingly, as no further issues are believed to remain outstanding in the present application, it is believed that this application is clearly in condition for formal allowance and an early and favorable action to this effect is earnestly and respectfully requested.

Respectfully submitted,

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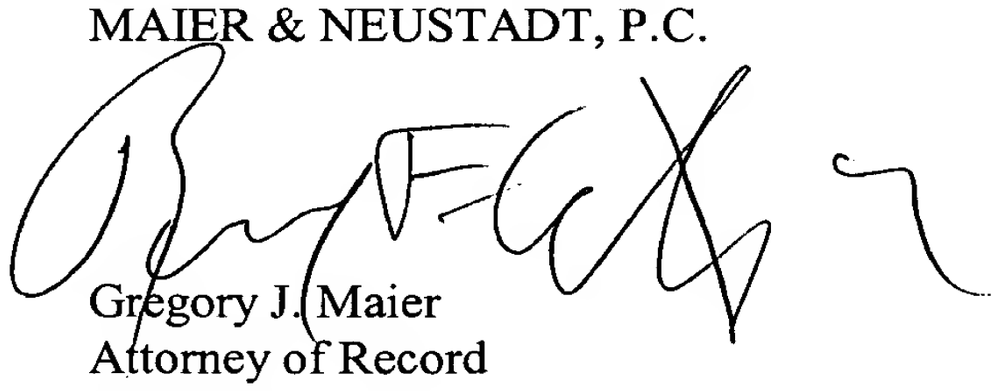

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